9/30/3

INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)	Docket No.: YOR920030139US1 Serial No.: 10/674,331 Applicant(s): Chirag S. PATEL Filing Date: Group:

U.S. PATENTS

Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a

OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)

C.C.	S. Kiyono et al, Consideration of Chip Circuit Damages on DCS-FBGA Packages
C.C.	Wu, L., Wang, Y. P., Hsiao C. S., "Innovative Stack-Die Package – S2BGA
C.C.	M. Sunohara et al., Development of Wafer Thinning and Double-Sided Bumping
C.C.	Technologies for the Three-dimensional Stacked LSI, all three presented at
	52nd Electronic Components and Technology Conference, May 2002, San Diego, CA
C.C.	Intel Stacked Chip Scale Packaging Products, available at
	http://www.intel.com/design/flcomp/prodbref/298051.htm

Examiner's Signature: [signature] Date Considered: 11/8/05

Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).